Fig. 1

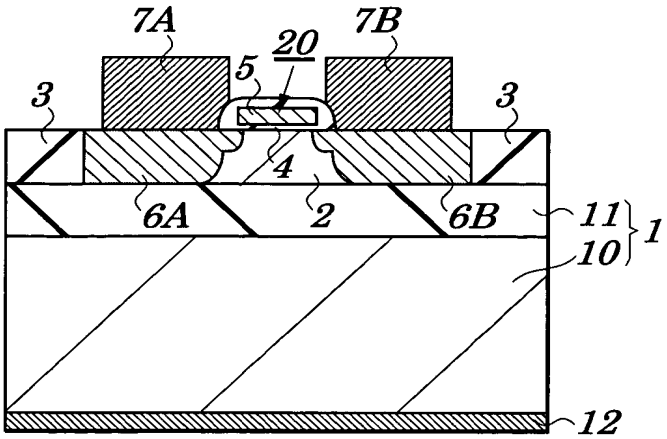
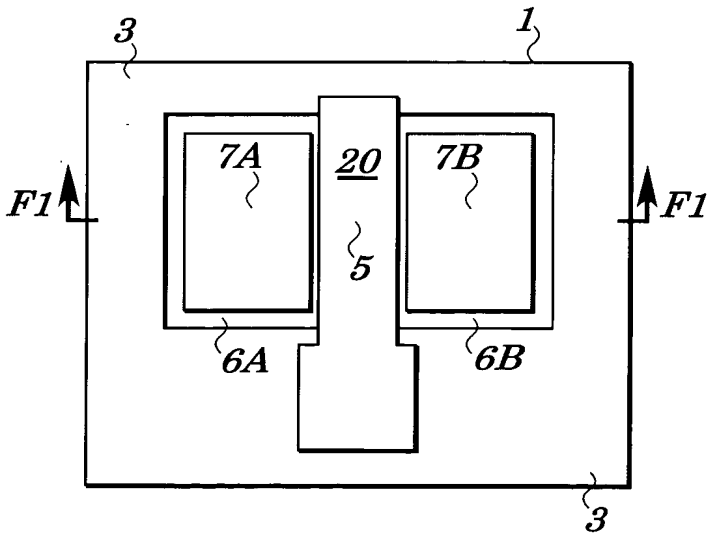


Fig. 2



10021 /26100

Fig. 3

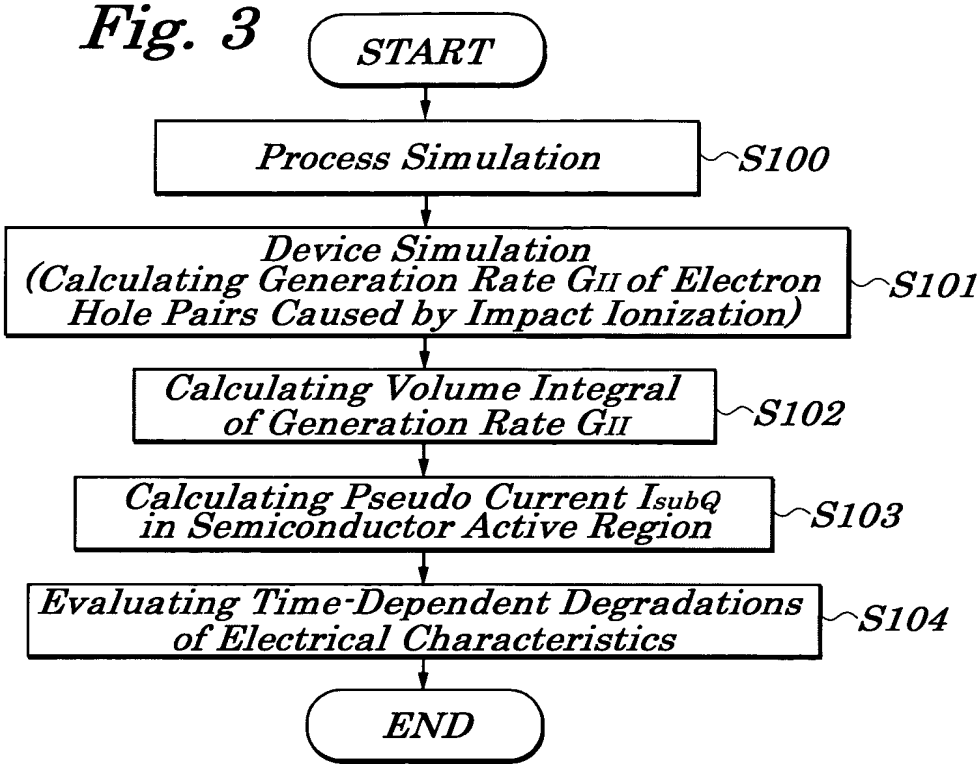


Fig. 4

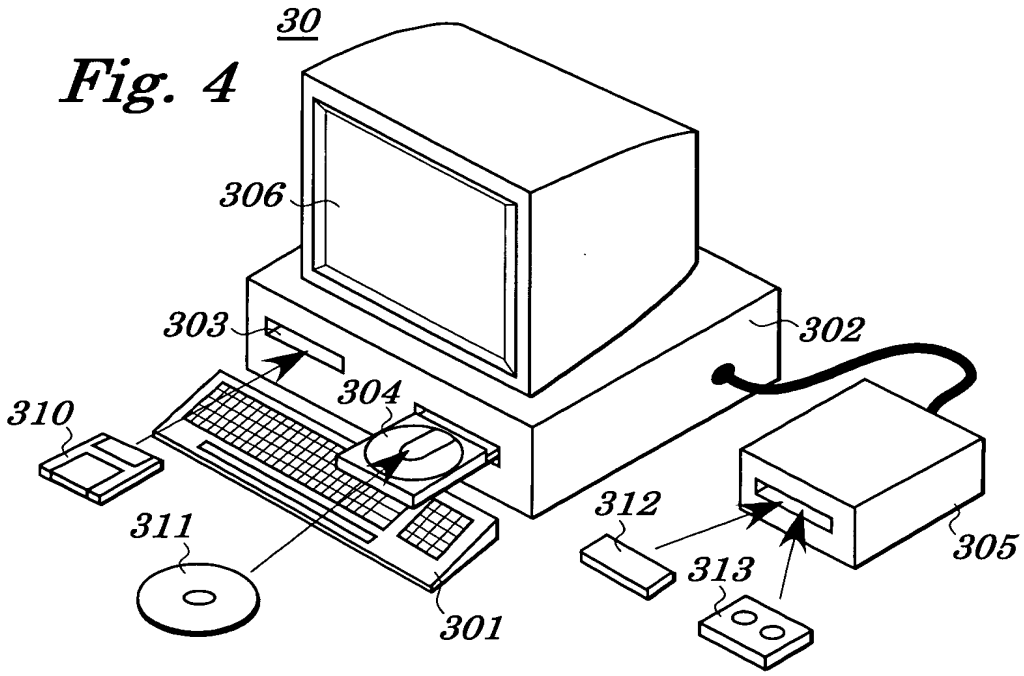


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Fig. 5

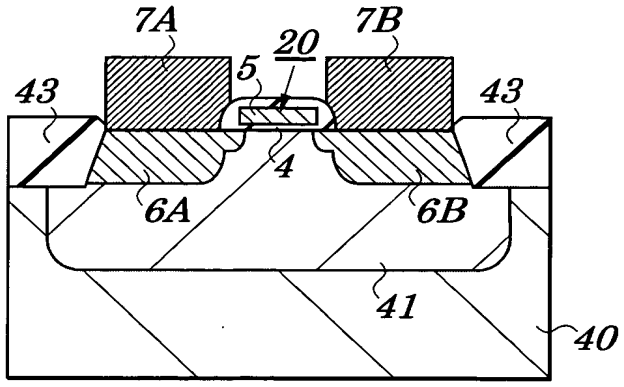

Fig. 6

Id[A] / IsubQ/Idratio	0.0001	0.0002	0.0005	0.001	0.002
0.01	5.0E-08	1.3E-07	4.8E-07	1.3E-06	3.3E-06
0.02	7.5E-07	2.0E-06	7.1E-06	1.9E-05	5.0E-05
0.05	2.7E-05	7.0E-05	2.5E-04	6.7E-04	1.8E-03
0.1	4.0E-04	1.1E-03	3.8E-03	1.0E-02	2.6E-02
0.2	5.9E-03	1.6E-02	5.7E-02	1.5E-01	3.9E-01

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Fig. 7

I_{subQ}/Id ratio \ Id[A]	0.0001	0.0002	0.0005	0.001	0.002
0.01	4.7E-08	1.3E-07	4.9E-07	1.2E-06	3.6E-06
0.02	7.0E-07	1.9E-06	7.3E-06	1.9E-05	5.3E-05
0.05	2.5E-05	6.7E-05	2.6E-04	6.6E-04	1.9E-03
0.1	3.7E-04	1.0E-03	4.0E-03	1.1E-02	2.5E-02
0.2	5.8E-03	1.5E-02	5.9E-02	1.4E-01	4.0E-01

Fig. 8

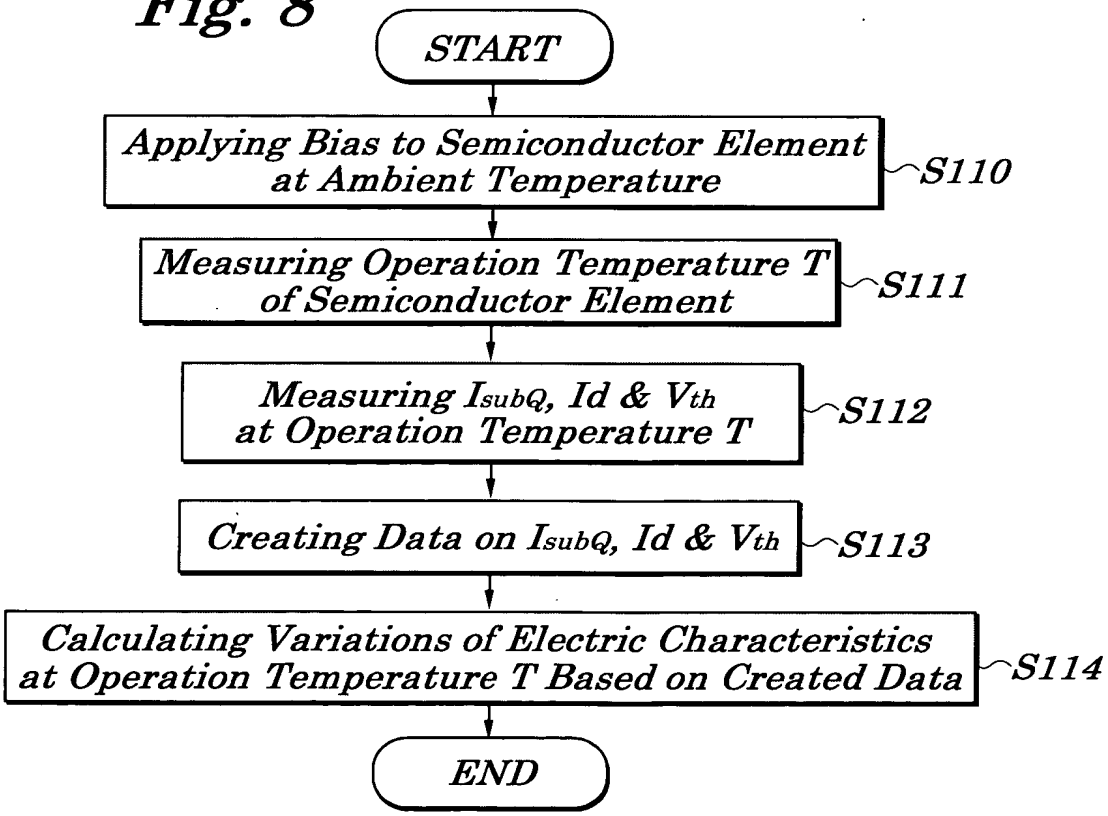

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Fig. 9

IsubQ/Idratio \ Id[A]	0.0001	0.0002	0.0005	0.001	0.002
0.01	8.4E-08	2.3E-07	8.8E-07	2.3E-06	5.5E-06
0.02	1.3E-06	3.4E-06	1.3E-05	3.4E-05	8.1E-05
0.05	4.5E-05	1.2E-04	4.7E-04	1.2E-03	2.9E-03
0.1	6.7E-04	1.7E-03	6.0E-03	1.6E-02	4.1E-02
0.2	9.8E-03	2.6E-02	9.0E-02	2.5E-01	6.6E-01

Fig. 10

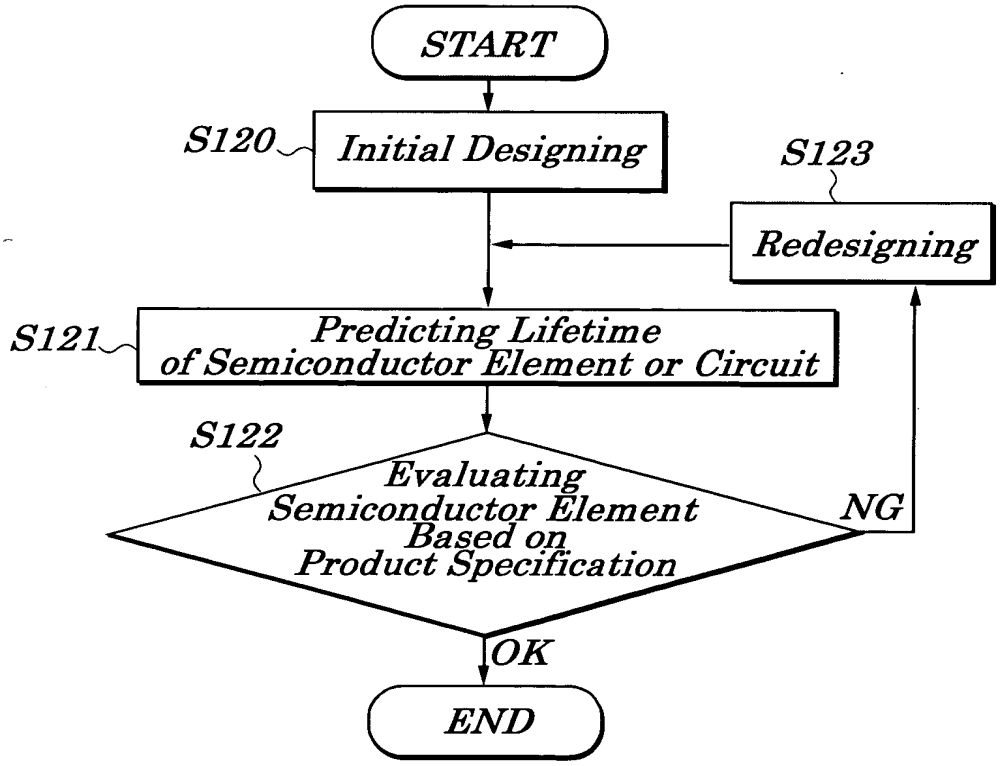

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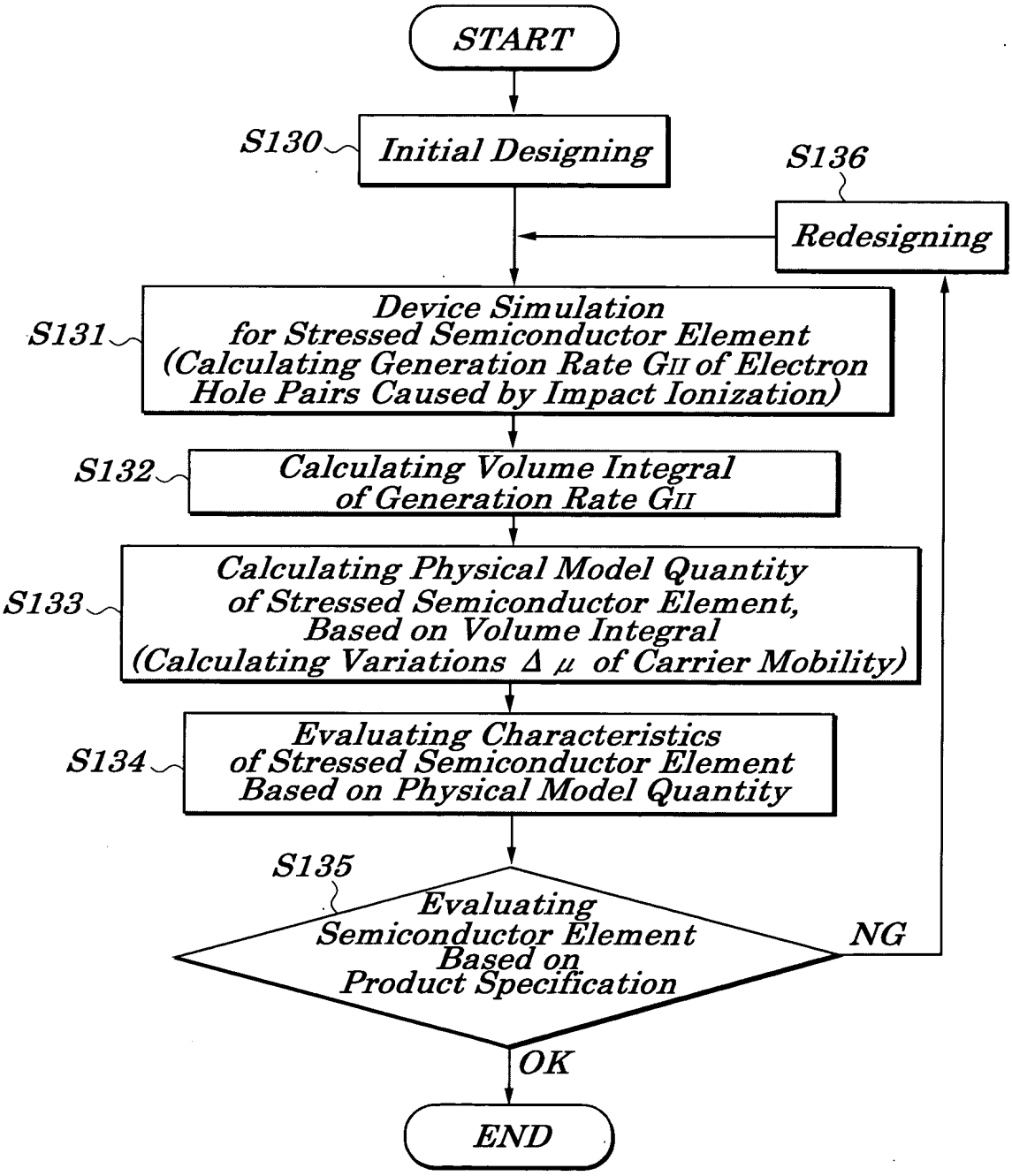
Fig. 11



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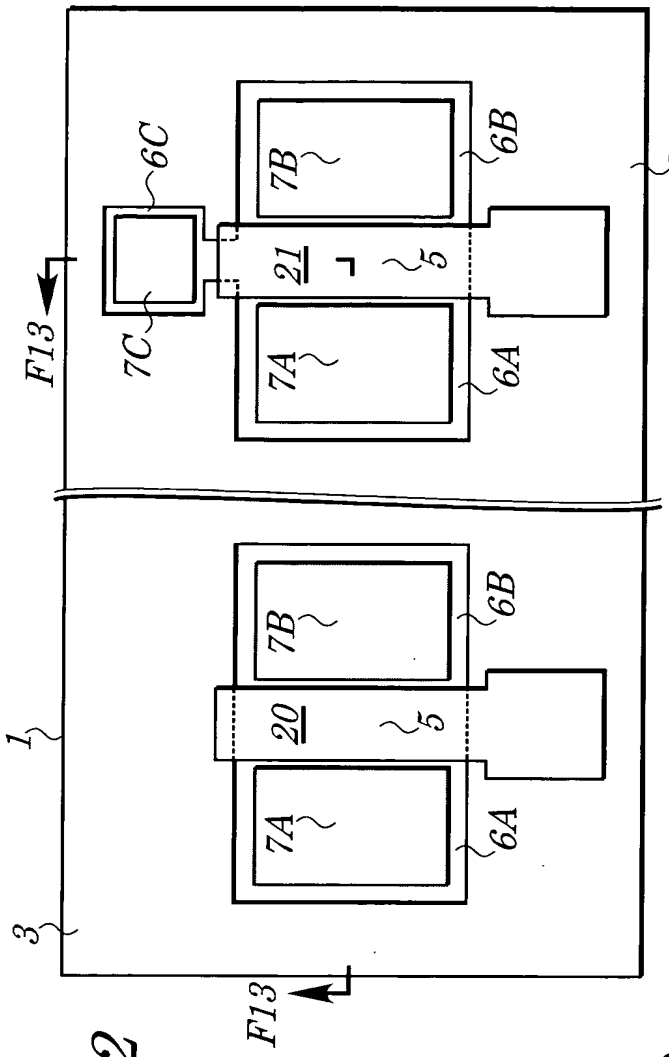

Fig. 12

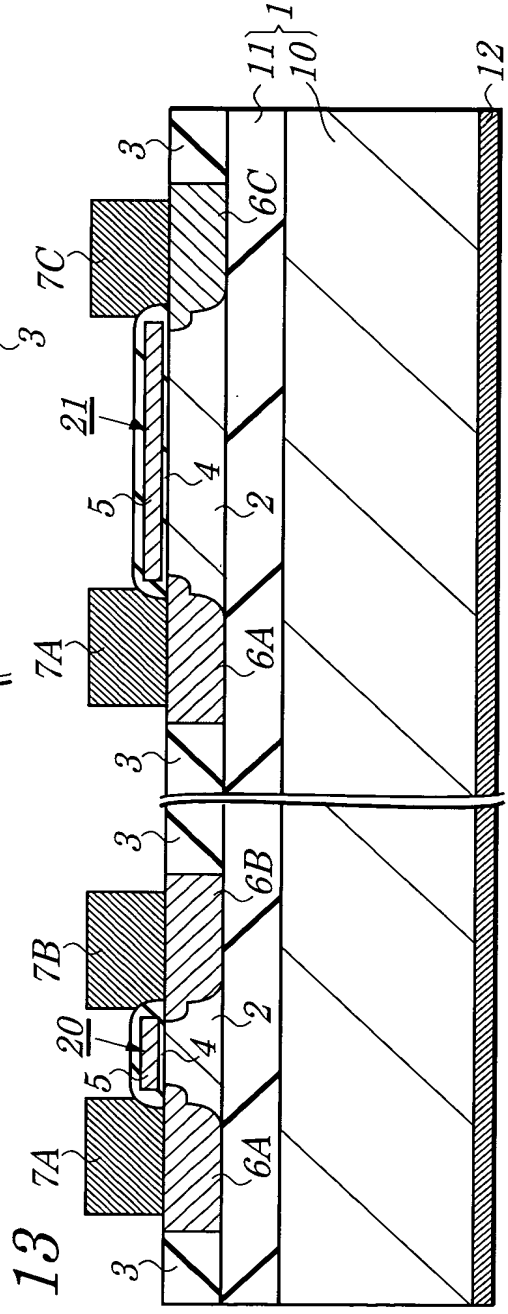

Fig. 13

Fig. 14

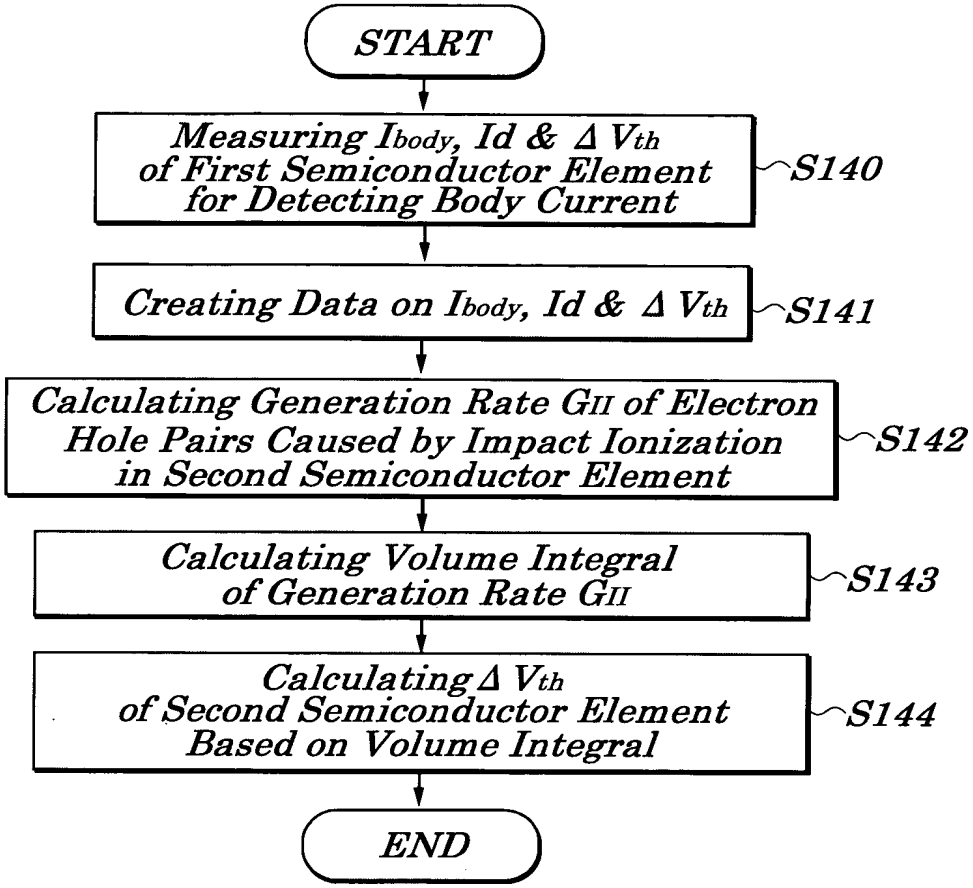
START
Measuring Ibody, Id & Δ Vth of First Semiconductor Element for Detecting Body Current
S140
Creating Data on Ibody, Id & Δ Vth
S141
Calculating Generation Rate GII of Electron Hole Pairs Caused by Impact Ionization in Second Semiconductor Element
S142
Calculating Volume Integral of Generation Rate GII
S143
Calculating Δ Vth of Second Semiconductor Element Based on Volume Integral
S144
END

FIG. 1

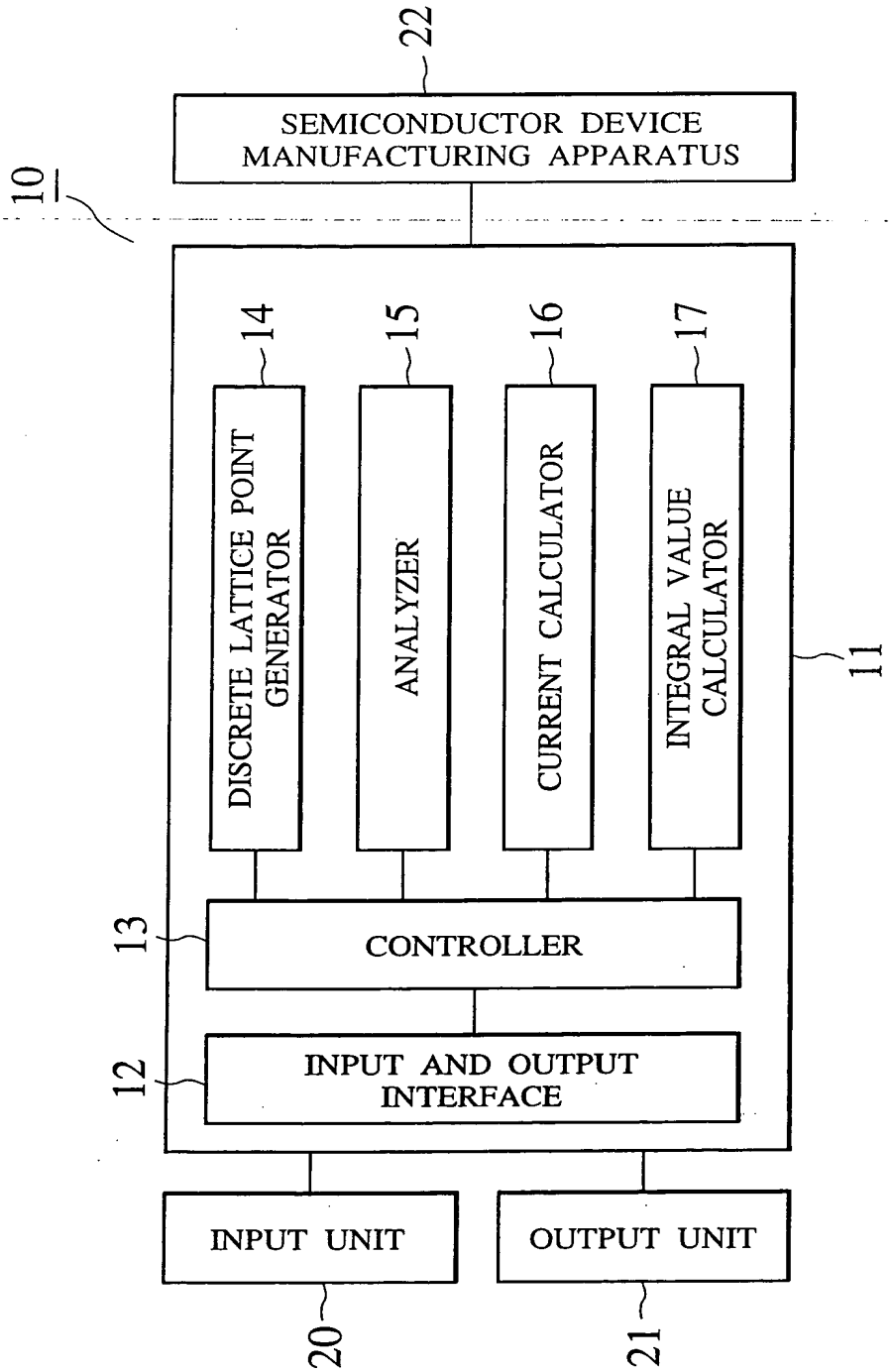
22
SEMICONDUCTOR DEVICE MANUFACTURING APPARATUS
10
14
15
16
17
DISCRETE LATTICE POINT GENERATOR
ANALYZER
CURRENT CALCULATOR
INTEGRAL VALUE CALCULATOR
11
13
CONTROLLER
12
INPUT AND OUTPUT INTERFACE
INPUT UNIT
OUTPUT UNIT
20
21

FIG. 2

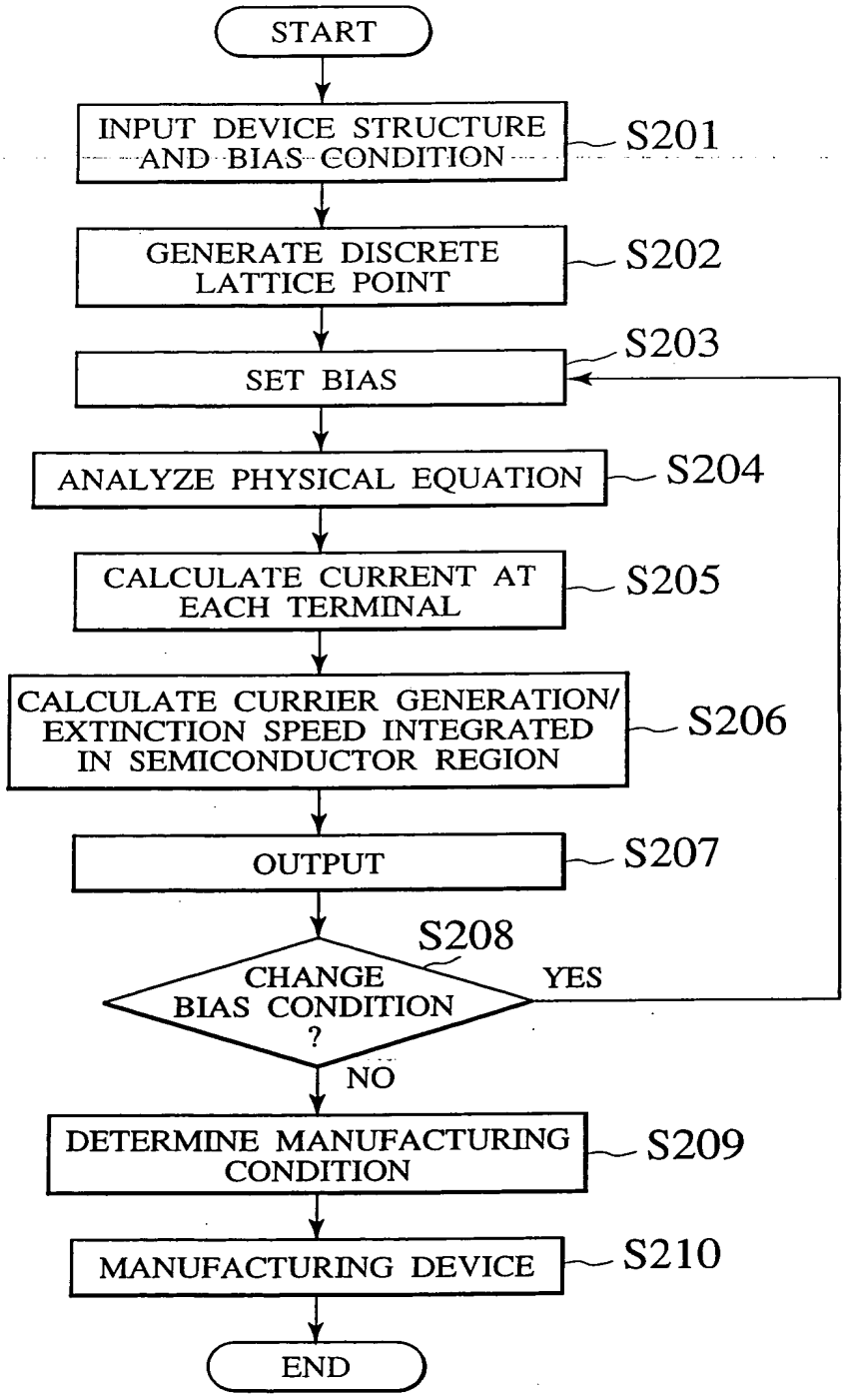
START
INPUT DEVICE STRUCTURE AND BIAS CONDITION
S201
GENERATE DISCRETE LATTICE POINT
S202
S203
SET BIAS
ANALYZE PHYSICAL EQUATION
S204
CALCULATE CURRENT AT EACH TERMINAL
S205
CALCULATE CURRIER GENERATION/ EXTINCTION SPEED INTEGRATED IN SEMICONDUCTOR REGION
S206
OUTPUT
S207
S208
CHANGE BIAS CONDITION ?
YES
NO
DETERMINE MANUFACTURING CONDITION
S209
MANUFACTURING DEVICE
S210
END

FIG. 3

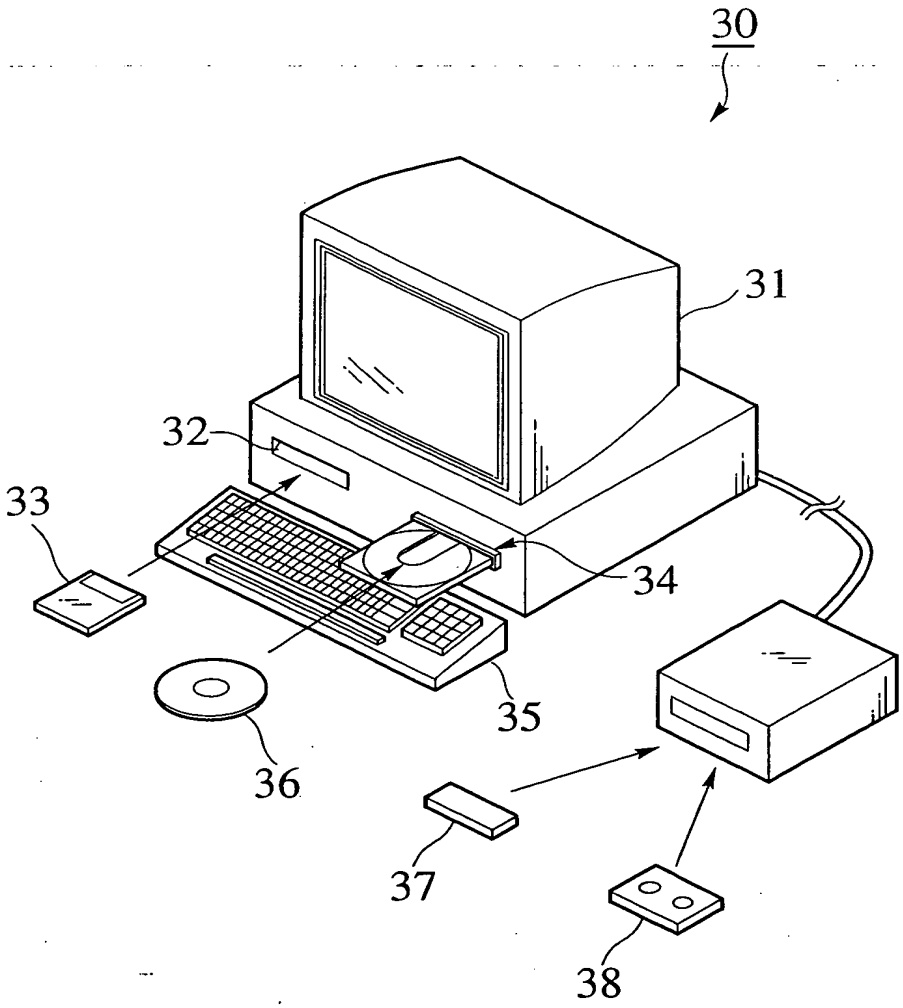

FIG. 4

(DEVICE STRUCTURE)	
IMPURITY CONCENTRATION OF P-TYPE SUBSTRATE	$3\times10^{17}cm^{-3}$
GATE OXIDE FILM THICKNESS	6nm
GATE ELECTRODE	N-TYPE POLYSILICON
GATE LENGTH	0.3 μm
SOURCE/DRAIN DIFFUSION LAYER MAXIMUM CONCENTRATION	$1\times10^{20}cm^{-3}$
SOURCE/DRAIN DIFFUSION LAYER JUNCTION DEPTH	0.08 μm
DEVICE WIDTH	1 μm

FIG. 5A

	NO GR	SRH ONLY	II ONLY	BBT ONLY	ALL
SOURCE CURRENT	4.08E-17	1.38E-17	1.37E-17	4.17E-19	1.29E-18
DRAIN CURRENT	4.07E-17	6.78E-17	6.72E-17	9.45E-14	9.63E-14
SUBSTRATE CURRENT	3.37E-18	9.41E-18	1.72E-18	9.45E-14	9.62E-14

FIG. 5B

SOURCE CURRENT	1.29E-18
DRAIN CURRENT	9.63E-14
SUBSTRATE CURRENT	9.62E-14

MECHANISM	VOLUME INTEGRAL VALUE X PRIME CHARGE
J_{SRHn}	1.50E-17
J_{IIn}	1.68E-15
J_{BBTn}	9.45E-14

FIG. 6A

	NO GR	SRH ONLY	II ONLY	BBT ONLY	ALL
SOURCE CURRENT	4.08E-04	4.48E-04	4.48E-04	4.48E-04	4.48E-04
DRAIN CURRENT	4.08E-04	4.48E-04	4.48E-04	4.48E-04	4.48E-04
SUBSTRATE CURRENT	4.66E-18	1.59E-17	4.33E-08	4.66E-18	4.33E-08

FIG. 6B

SOURCE CURRENT	4.48E-04
DRAIN CURRENT	4.48E-04
SUBSTRATE CURRENT	4.33E-08

MECHANISM	VOLUME INTEGRAL VALUE X PRIME CHARGE
J_{SRHn}	4.78E-14
J_{IIn}	4.33E-08
J_{BBTn}	0.00E+00

FIG. 7A

$$\frac{\delta n}{\delta t} = \frac{1}{q}\vec{\nabla} \cdot \vec{J_n} + GR_n$$

FIG. 7B

$$GR_n = GR_{SRHn} + GR_{IIn} + GR_{BBTn}$$

FIG. 7C

$$A_{SRHn} = \int_{Si} GR_{SRHn} dv$$

FIG. 7D

$$A_{IIn} = \int_{Si} GR_{IIn} dv$$

FIG. 7E

$$A_{BBTn} = \int_{Si} GR_{BBTn} dv$$

FIG. 7F

$$J_{SRHn} = q \int_{Si} GR_{SRHn} dv$$

FIG. 7G

$$J_{IIn} = q \int_{Si} GR_{IIn} dv$$

FIG. 7H

$$J_{BBTn} = q \int_{Si} GR_{BBTn} dv$$